UNIVERSITY OF TWENTE.

Exam Computer Systems/Computer Architecture and Organisation

Bachelor 2nd year, EE and CS, EWI

Module/course code: Computer Systems 201400210(CS) / 201400217(EE)
Date: 27 September 2019
Time: 13:45-15:30 *(+25% for students who may use extra time)*
Module-coördinator: A.B.J. Kokkeler
Instructor: E. Molenkamp / A.B.J. Kokkeler

Type of test: Closed book
Allowed aids during the test: Writing materials, simple calculator

27 questions on 8 pages and 4 pages with the ARC documentation

Instructions for this examination:

1. Scientific or graphical calculators, laptops, mobile phones, books etc. are not allowed. Put those in your bag now (and **switched off**)!
2. Write your answers on this paper, in the provided boxes , and hand in this exam **and** the multiple choice form (even when you did not answer any questions).
3. All multiple choice questions have exactly one correct answer; place an X in the correct box and copy the answer to the multiple choice form.
4. The multiple choice form is scanned and automatically corrected. Make sure to fill in that form completely (except for the "docent / teacher" part).
5. For grading the exam, correction for guessing is used.
6. Exactly 1 answer is correct. No answer given is counted as an incorrect answer.
7. Write your name, student number and educational programme at the bottom of this page.
8. The documentation refers to the ARC processor. If a problem indicates that it is about the **subset ARC** processor then only the instructions listed in figure 5-2 (documentation page 2) may be used.

Logic symbols: **not a** is also represented as $\overline{a}$, **a'**, **!a**, **#a**
a and b is also represented as **a.b**, **a&b**
a or b is also represented as **a + b**
a xor b is also represented as $a \oplus b$

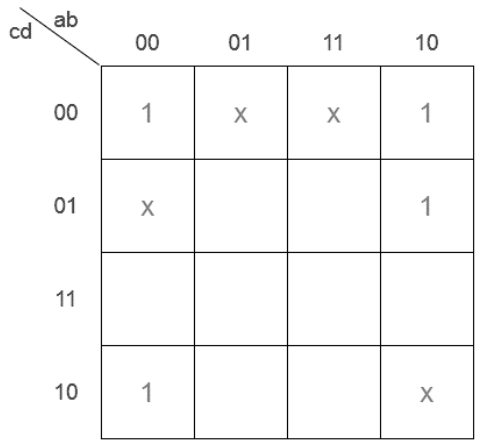
(please underline your family name (i.e., the name on your student card), so that we know how to sort))

Name: .....

Student number: .....

Educational programme (EE, TCS, ..): .....

Question 1



cd \ ab	00	01	11	10
00	1	x	x	1
01	x			1
11				
10	1			x

What is the simplified Boolean equation for this Karnaugh map?
X denotes a don't care term and the fields that are not filled in are 0.

a☐ b'.d'

b☐ b'.d' + b'.c'

c☐ b'.d' + a'.b'.c'.d'

d☐ b'.d' + b'.c'+ c'.d'

Question 2

What is the simplified Sum of Product of the Boolean expression
(a + b).(a' + b + c)

a☐ a.b + c

b☐ b.(a'+ c)

c☐ b + a.c

d☐ a.c + a.b + a'.b

Question 3

What is the minterm expansion of
F(P,Q,R) = P.Q + Q.R'+ P.R'

a☐ $\sum m(2,4,6,7)$

b☐ $\sum m(0,1,3,5)$

c☐ $\sum m(0,1,6,7)$

d☐ $\sum m(2,3,4,5)$

Question 4

What is the minimum number of gates required to implement the Boolean function (A.B+C) if only 2-input NAND gates are used?

a☐ 2

b☐ 3

c☐ 4

d☐ 5

Question 5

What is the hexadecimal representation of octal 3657 ?

a☐ 7AF

b☐ D78

c☐ D71

d☐ 32F

Question 6

Given is a normalized floating point representation in base 2. The bit pattern from left to right is: Sign bit: 1 bit (1 is negative, 0 is positive), Exponent field: 7 bits in excess 64, Fraction field: 8 bits (not included is the hidden bit). Point is right of hidden bit.
Only when the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

What is the hexadecimal representation of decimal $8\frac{5}{8}$ (use rounding style truncation) in this floating point representation?

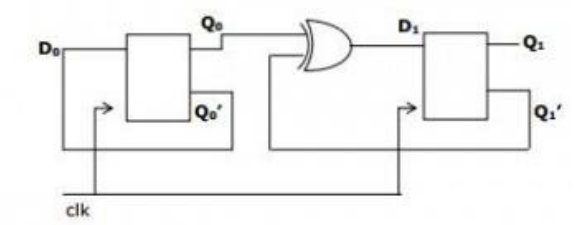
a☐ 4314
b☐ 40A0
c☐ 2F1A
d☐ 2A13

Question 7

Given the floating point representation as defined in question 6. What is the maximum positive decimal value that can be represented?

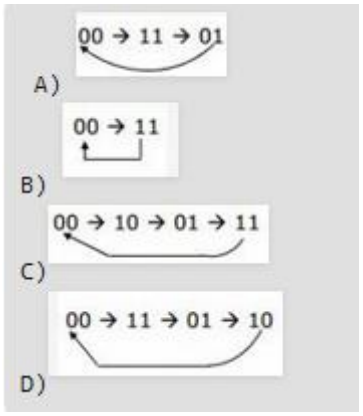
a☐ 2^{126}
b☐ 2^{127}
c☐ $2^{63}(1-2^{-9})$
d☐ $2^{63}(2-2^{-8})$

Question 8

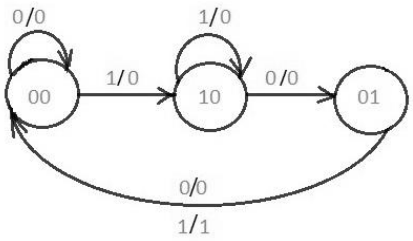


The Data flip-flops in this schematic are positive edge triggered. Each state is designated as a two bit string Q_0Q_1. Let the initial state be 00.
Note: Q_0 is left bit of the state.
What is the state transition sequence?

a☐
b☐
c☐
d☐



Question 9



This Finite State Machine is realized with 2 data flip-flops (Q_1Q_0) and combinational logic. **Note: Q_1 is left bit of the state**. The input is X and the output is Y. For the state Q_1Q_0=11 the behavior is undefined. What is the Boolean equation for the data input (D_1) of Q_1?

a☐ $D_1 = Q_1.X + Q_1'.Q_0'$

b☐ $D_1 = Q_0 + Q_1'.X$

c☐ $D_1 = Q_1'.Q_0'$

d☐ $D_1 = Q_0' .X$

Question 10

Given is the Finite State Machine of question 9. What is a Boolean equation for the output Y?

a☐ $Y = (Q_1' + Q_0).X$

b☐ $Y = Q_1.X$

c☐ $Y = Q_1'.Q_0.X$

d☐ $Y = Q_1'.Q_0.+ X$

Question 11

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The table above is a 2 bit saturating up-counter. The counter is built as a synchronous sequential circuit using D flip-flops. The Boolean equations for the data input D_1 (input of flip-flop Q_1) and D_0 (input of flip-flop Q_0) are:

a☐ $D_1=Q_1 + Q_0$ and $D_0=Q_1+Q_0'$

b☐ $D_1=Q_1'. Q_0$ and $D_0=Q_1'+Q_0'$

c☐ $D_1=Q_1 + Q_0'$ and $D_0=Q_1+Q_0$

d☐ none of these

Question 12

The worst case delay of the full adders used in a carry ripple adder is 2 ns (from any input to any output). What is approximately the worst case delay of an N bit ripple carry adder?

a☐ $\log_2(N) \times 2$ ns

b☐ $N^2 \times 2$ ns

c☐ $N \times 2$ ns

d☐ None of these

Question 13

The timing properties of a Data flip-flop are: setup time (Tsu) is 3 ns, Hold time (Th) is
-1 ns, clock to output delay (Tco) is 2.5 ns.
What is correct?

a☐ For a correct behavior the data input must be stable 3 ns before until 1 ns before the active edge of the clock.

b☐ The output is stable 1.5 ns after the active edge of the clock.

c☐ A negative time for the hold time is not valid.

d☐ none of these

Question 14

What is an ARC assembly instruction that has as behavior that the contents of %r1 becomes decimal -1?
Representation is twos complement.

a☐ orn %r0, %r0, %r1

b☐ ld [%r0-1], %r1

c☐ sethi -1, %r1

d☐ None of these

Question 15

```
.begin
.org 0
        ld[x], %r1
        orn %r0, %r1, %r1
        addcc %r1,1,%r1
        bneg over
        st %r1, [x]
over:   halt
x:      -10
.end
```

a☐ In main memory the contents at decimal address 24 has decimal value 10.

b☐ The decimal value of label *over* is decimal 5.

c☐ The instruction *halt* is at hexadecimal address 16.

d☐ None of these.

After the execution of this program, what is correct?

Question 16

```
.begin
.org 0
sethi   series,%r1
        srl     %r1,10,%r1
        addcc   %r0, 0, %r11
lp:     ld      [%r1], %r10
        addcc   %r10,%r0,%r0
        be      rdy
        addcc   %r10,%r11,%r11
        ????????
        ba      lp
rdy:    halt
series: 1,2,3,4,0
        .end
```

a☐ `srl %r1, 4, %r1`

b☐ `srl 1, %r1, %r1`

c☐ `addcc %r1, 4, %r1`

d☐ `addcc %r1, 1, %r1`

This program should accumulate the 32-bit integer values in the list with start address *series*. The list is terminated with decimal 0. What instruction should be inserted on the line with **????????**

Question 17

The ARC processor is extended with instruction FUN. The micro program of the execution phase of FUN is given below.

address	A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
1792	-	1	%r0	0	%temp0	0	0	0	addcc	next address	-
1793	-	1	-	-	%temp1	0	0	0	lshift2	Next address	-
1794	%temp0	0	%temp1	0	-	1	0	0	addcc	Jump	2047

What is correct?

a☐ After execution of FUN the contents of %temp0 is always 0

b☐ The contents of %temp0 and %temp1 is always the same

c☐ The RTL behavior of this instruction is: $R[rd] \leftarrow 3 \times R[rs1]$

d☐ The RTL behavior of this instruction is: $R[rd] \leftarrow 5 \times R[rs1]$

Question 18

What is the bit pattern of the *field op3* in the machine code of an ARC instruction when the start address in the micro store is decimal 1792?

a☐ 000000

b☐ 000001

c☐ 000010

d☐ None of these

Question 19

What is correct?

a☐ Memory-mapped I/O uses a single address space to address both memory and I/O devices.

b☐ A processor that supports memory-mapped I/O has different read and write instructions for IO and memory.

c☐ A computer based on the *von Neumann model* has no Control Unit.

d☐ The register in a processor with name *program counter* counts the number of instructions executed.

Question 20

Given two processors with word size of 32 bits and a byte-organized memory. Processor A uses Little-Endian addressing and Processor B uses Big-Endian addressing. Processor A writes data to memory and Processor B reads data from the address written by Processor A. What is read by Processor B when Processor A wrote (hex) 89AB?

a☐ 89AB

b☐ BA98

c☐ AB89

d☐ A98B

Question 21

What is correct?

a☐ In a modern processor the programmed I/O technique is always used for reading the keyboard.

b☐ In the interrupt I/O technique the processor interrupts the connected devices.

c☐ In the interrupt I/O technique the processor is polling for an interrupt of a device.

d☐ DMA is a technique for transferring data between main memory and external device with minimal involvement of the CPU.

Question 22

Consider the following interrupt scenario and assume an interrupt **cannot** suspend other interrupts:

Task	Service time	Maximum allowed latency	Maximum Frequency
A	10 ms	15 ms	1/(100 ms)
B	20 ms	35 ms	1/(200 ms)
C	40 ms	200 ms	1/(400 ms)
D	50 ms	200 ms	1/(500 ms)

What is correct?

a☐ Maximum allowed latencies for all the tasks are met

b☐ Task D can prevent task A being serviced in time

c☐ Task A can prevent task C being serviced in time

d☐ None of the these

Question 23

An embedded computer system has a physical address space of 8 MB. The memory is byte addressable. I/O mapped I/O is used. When pin *M/in* is low the I/O devices are selected. The system contains an Ethernet controller, video-RAM and a Wifi controller according to the following specifications concerning addressing.

Ethernet controller:	1 MB at the lowest addresses of the address range.
Video-RAM:	256 KB directly following the area for the Ethernet controller.
Wifi controller:	4 MB at the highest addresses of the address range.
Shadowing is not allowed.	

The signals to select the different areas are respectively *SelEth*, *SelVideo* en *SelWifi*.
The bits of the address bus are $A_{N-1}..A_0$ (N is number of address lines, right most bit has index 0)

What is the equation for *SelEth* ?

a☐ *SelEth* = $!A_{22}$ & $!A_{21}$ & $!A_{20}$ & A_{19} & !M/in

b☐ *SelEth* = $!A_{22}$ & $!A_{21}$ & $!A_{20}$ & !M/in

c☐ *SelEth* = $!A_{23}$ & $!A_{21}$ & $!A_{20}$ & A_{19} & !M/in

d☐ *SelEth* = $!A_3$ & $!A_2$ & $!A_1$ & A_0 & !M/in

Question 24

See question 23.

What is the equation for *SelVideo* ?

a☐ *SelVideo* = $!A_{22}$ & $!A_{21}$ & A_{20} & $!A_{19}$ & $!A_{18}$ & $!A_{17}$ &!M/In

b☐ *SelVideo* = $!A_{22}$ & $!A_{21}$ & A_{20} & $!A_{19}$ & $!A_{18}$ & !M/In

c☐ *SelVideo* = ($!A_{22}$ + $!A_{21}$ + A_{20} + $!A_{19}$ + $!A_{18}$ +$!A_{17}$) & !M/In

d☐ *SelVideo* = $!A_{22}$ & $!A_{21}$ & A_{20} & $!A_{19}$ & !M/In

Question 25

A 16-bits microprocessor has an on-chip primary cache with the following characteristics:

Address space: 4 MB, Byte-addressing
Primary cache: Size: 16 KB (excluding tags)
Slotsize: 512 B
Organisation: 4-way set-associative

For the primary cache, a byte-address is split into parts that are used for, respectively, comparison with the *tag* in the cache, selection of a *set in the cache*, selection of a *word in a slot* and selection of a *byte in a word*. Note: the right most bit has number 0.

What are the bit numbers of the address that selects **set in the cache**?

a☐ 13, 12, 11, 10, 9

b☐ 12, 11, 10

c☐ 10, 9, 8

d☐ 11, 10, 9

Question 26

See question 25

What are the bit numbers of the address that selects **word in a slot**?

a☐ 7, 6, 5, 4, 3, 2, 1

b☐ 8, 7, 6, 5, 4, 3, 2, 1

c☐ 9, 8, 7, 6, 5, 4, 3, 2, 1

d☐ 9, 8, 7, 6, 5, 4, 3, 2

Question 27

A dynamic RAM chip is organised as follows: 64M x 2 bits. Using multiple of these chips, a memory module of in total 1024 Mbytes has to be built. The word width is 32 bits.
How many columns (to establish the correct word width) and how many rows does the memory module contain?

a☐ columns: 16 rows: 8

b☐ columns: 16 rows: 4

c☐ columns: 32 rows: 4

d☐ columns: 8 rows: 8