

Exam Computer Systems/Computer Architecture and Organisation

Bachelor 2nd year, EE and CS, EWI

Module/course code: Computer Systems 201400210(CS) / 201400217(EE)

Date: 25 September 2015

Time: 13:45-15:30 (*+25% for students who may use extra time*)

Module-coördinator: A.B.J. Kokkeler

Instructor: E. Molenkamp / A.B.J. Kokkeler

Type of test:

- Closed book

Allowed aids during the test:

- Writing materials, simple calculator

Attachments:

- ARC processor Documentation

Additional remarks:

- 13 questions on 10 pages

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Computer architecture and organization

Friday 25 September 2015, 13.45 – 15.30

13 problems, 10 pages, 4 pages with the ARC documentation

Instructions for this examination:

1. Answer the questions only in the designated locations on this form.
2. Write your name and student number on each page of this exam
3. Furthermore fill in your name, educational programme and student number below on this page.
4. Hand in all pages of this exam.
5. You may only use writing material and a simple calculator.
6. The documentation refers to the ARC processor. If a problem indicates that it is about the **subset ARC** processor then only the instructions listed in figure 5-2 (documentation page 2) may be used.

Name:

Student number:

Educational programme:

Question 1 (2 points)

$$f(A, B, C, D) = \sum (1,9,10,11) + \sum_d (2,8)$$

Give a minimal Boolean equation in sum-of-products for f

$$A.!B + !B.!C.D$$

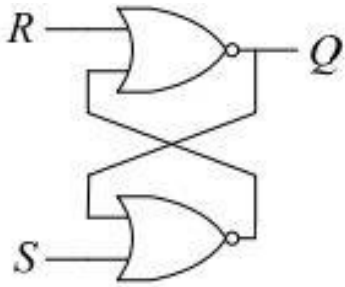
Question 2 (1 points)

A full adder has three inputs: A, B, Ci (Carry in) and two outputs: S (sum) and Co (Carry out). Give a minimal Boolean equation for S. You are allowed to only use NOT and XOR functions.

$$S = A \oplus B \oplus C$$

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Question 3 (1 + 1 = 2 points)



Is this synchronous sequential logic?

No (it is asynchronous)

Give a minimal Boolean equation in sum-of-products for Q

$$Q = !R.S + !R.Q$$

Question 4 (1 + 1 = 2 points)

Given is a normalized floating point representation in base 2. The bit pattern from left to right is:

- Sign bit: 1 bit (1 is negative, 0 is positive),
- Exponent field: 6 bits in excess 11,
- Fraction field: 5 bits (not included is the hidden bit). Point is right of hidden bit.

When the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

a) What is the bit representation of decimal $-2\frac{5}{8}$ (use rounding style is truncation)

Sign bit: 1
Exponent field: 001100
Fraction field: 01010

b) What is the smallest positive number (greater than 0) that can be represented (answer in powers of 2 or decimal floating point representation with at least 5 significant digits)?

$$1 \times 2^{-10} = 2^{-10} \text{ or } 9.76563 \times 10^{-4}$$

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Question 5 (1 points)

What is the machine code (in hexadecimal format) of the ARC instruction:

`st %r3, [%r4 + 2]`

C6212002

Question 6 (3 points)

Given is an array `series` that contains 32 bit signed numbers. The end of the array is indicated with the integer value 0. Write an efficient assembly program that counts the number of odd numbers.

This number must be stored in `%r11`. **Add comment!**

(Tip: what is the property of the bit patterns of odd numbers?)

```
.begin
.org 0
sethi series,%r1
srl   %r1,10,%r1           ! %r1 contains address of series.

        addcc %r0, 0, %r11           ! %r11 bevat aantal oneven getallen
lp:     ld    [%r1], %r10           !
        addcc %r10,%r0,%r0         ! check zero
        be   rdy
        andcc %r10,1,%r0          ! filter LSB bit; odd?
        be   nxt
        addcc %r11,1,%r11         ! aantal++
nxt:    addcc %r1,4,%r1           ! %r1 = %r1 + 4
        ba   lp
rdy:    halt
series: 1,3,4,5,9,8,-7,0
.end
```

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Question 7 (2 + 1 + 1 = 4 points)

The state table of a synchronous state machine is:

Present state	Next state		Z	
	\bar{X}	X	\bar{X}	X
S0	S0	S1	0	1
S1	S0	S1	1	0

For the encoding of this state machine one D flip-flop is used (F) with encoding S0=0, S1=1.

a) Give a minimal SOP form for the data input of flip-flop F (i.e. $DF=f(X,F)$)

$$DF = X.$$

b) Give a minimal SOP form for the output Z

$$Z = !F.X + F.!X$$

c) Is this a MOORE or a MEALY machine?

Mealy; output depends on state and input

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Question 8 (1 + 1 + 1 = 3 points)

address	A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
1784	-	1	-	-	%temp0	0	0	0	lshift2	Next	-
1785	%temp0	0	-	1	-	1	0	0	add	Jmp	2047

The ARC processor is extended with the instruction FUN with start address 1784 (decimal) in the microstore. The number representation is twos complement.

FUN %rx, %ry, %rz with rs1=%rx1, rs2=%ry and rd=%rz

a) What is the bit pattern of field **op3** of the instruction?

op3 = 111110

b) Which status bits (N, Z, V and C) are affected by instruction FUN?

lshift2 and add do not update the status; so status is unchanged

c) Give an RTL description of the function FUN (rd=f(rs1,rs2))

rd \leftarrow 4 \times rs1 + rs2

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Question 9 (3 x 1 = 3 points)

a) Explain in a few sentences Moore's law

Once every year (later once every 18 months, the number of transistors on a certain chip area doubles. .

b) Which concept exploits spatial and temporal locality?

Cache/Memory Hierarchy.

c) What is the general principle behind 'DMA' and what is the advantage

Principle:

The processor only initializes data transfer between an I/O device and memory while a separate device (the Direct Memory Access controller or DMA controller) actually transfers the data.

Advantage:

processor can do other tasks
Faster

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Question 10 (2 x 1 = 2 points)

A computer must service three devices whose interrupting frequencies, service times, and assigned priorities are given in the table below.

Device	Service time	Maximum Frequency	Priority
D1	20 ms	1/(200 ms)	3 (highest)
D2	40 ms	1/(400 ms)	2
D3	80 ms	1/(800 ms)	1 (lowest)

- a. Assuming a strong priority system (interrupts are enabled during interrupt handling), compute for each device the maximum time between service request and the completion of service for that device.

D1: 20.ms (D1 does not have to wait)

D2: 60 ms (D1 is busy (wait max 20ms) and 40ms for D2)

D3: 140 ms (Wait max for D1 (20ms) and D2 (40ms) + D3)

- b. What is the maximum percentage of the processor's time devoted to servicing D1?

10 % (D1 max 5 times/sec; 5*20ms is 100ms/sec)

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Question 11 (2 + 2 = 4 points)

An 'embedded' microcontroller is used for controlling a heating system. The microcontroller has 16 address pins (A0 until A15), an 8 bit data bus and makes use of 'I/O-mapped' I/O. For selecting the memory space, the M/In is asserted (made high), for selecting the I/O space, M/In is deactivated (made low). The memory system consists of ROM and RAM according the following specifications:

ROM: 4K Bytes at the lowest addresses of the address range

RAM: 8K Bytes at the highest addresses of the address range.

Shadowing is **not** allowed.

The select lines for these areas are respectively *SeIROM* and *SeIRAM*. These select lines are a function of a selection of address lines and the signal M/In.

a) Give the **minimal** expression for *SeIROM* (as a function of the addresslines and M/In).

$$\text{SeIROM} = \neg A_{15} \& \neg A_{14} \& \neg A_{13} \& A_{12} \& M/\text{In}$$

b) Give the expression for *SeIRAM* (as a function of the addresslines and M/In).

$$\text{SeIRAM} = A_{15} \& A_{14} \& A_{13} \& M/\text{In}$$

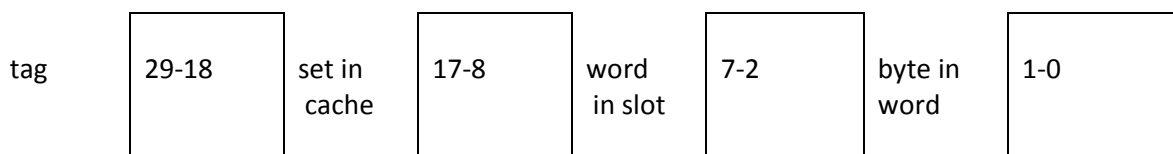
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Question 12 (1 + 1 + 1 + 1 = 4 points)

A 32-bits microprocessor has an on-chip primary cache with the following characteristics:

Address space: 1 GB, Byte-addressing
Primary cache: Size: 1 MB (excluding tags)
Slot size: 256 B
Organisation: 4-way set-associative

For the primary cache, a byte-address is split into parts that are used for, respectively, comparison with the tag in the cache, selection of a set in the cache, selection of a word in a slot and selection of a byte in a word. Which bit numbers belong to each of these parts?



Question 13 (1 point)

A processor is connected to byte-addressable 2^{32} byte memory via a 64 bit databus. What are the addresses (in hexadecimal representation) of the lowest and highest words of the memory?

```
Lowest Address:  
  
00000000 H  
  
Highest Address: FFFFFFF8 H
```