**Computer architecture and organization** Friday 26 September 2014, 13.45 – 15.30

13 problems, 7 pages, 4 pages with the ARC documentation

Instructions for this examination:

1. Answer the questions only in the designated locations on this form.
2. Fill in your name, educational programme and student number on the first page.
3. Fill in your name at the odd pages.
4. Hand in all pages of this exam.
5. You may only use writing material and a simple calculator.
6. The documentation refers to the ARC processor. If a problem indicates that it is about the **subset ARC** processor then only the instructions listed in figure 5-2 (documentation page 2) may be used.

Name: .....

Student number: ..... Educational programme: .....

## Question 1 (2 points)

$$f(A,B,C,D) = \sum(5,8,13,15) + \sum_d(0,7,9,12)$$

Simplify function *f* in sum-of-products form

## Question 2 (1 points)

The ALU in the ARC processor, see figure 5-3 (Documentation ARC, page 1), has output "Set Condition Codes". When this output is 1 the PSR register is updated else the PSR register is not changed.
Give a simplified Boolean equation in SOP-form for this output.

Set Condition Codes =

## Question 3 (2 points)

A synchronous sequential system with clock *clk* and low active asynchronous reset input *rst* has input *X* and output *Y*.

The output *Y* is 1 when in the previous two clock cycles the input values of *X* are the same; otherwise the output *Y* is 0. When the reset is active the system is in the state: nothing detected and the output *Y* is 0.

An example (data samples at active edge of the clock from left to right)

```
rst: 0011111111111111
X:   --00001010111100 (- is don't care)
Y:   0000111000001110
```

Draw a minimal state diagram for this system.

## Question 4 (1 + 1 + 1 = 3 points)

Given is a normalized floating point representation in base 2. The bit pattern from left to right is:

- Sign bit: 1 bit (1 is negative, 0 is positive),
- Exponent field: 10 bits in excess 30,
- Fraction field: 121 bits (not included is the hidden bit). Point is left of hidden bit.

When the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

What is the bit pattern of the decimal number **-2.8**.

Sign:

Exponent field:

Fraction field:

Name: .....

## Question 5 (1 points)

Give the ARC assembly instruction 32 bits machine code (hex):

**C6004000**

## Question 6 (3 points)

```
        .begin
        .org 0
        sethi arr1, %r1
        srl %r1,10,%r1   ! %r1 begin address arr1
        sethi arr2, %r2
        srl %r2,10,%r2
        addcc %r0,%r0, %r3
loop:   ld[%r1+%r3], %r4
        ld[%r2+%r3], %r5
        addcc %r4,%r5,%r6
        st %r6, [%r2+%r3]
        addcc %r4,%r0,%r0
        be ready
        addcc %r3,4,%r3
        ba loop
ready:  st %r0, [%r2+%r3]
        halt
        .org 100
arr1:   12, -4, 9, 8, 0
        .org 200
arr2:   4, -5, 4, 4, 12, 3, 0
        .end
```

What are the differences in main memory before and after the execution of this program. ONLY report the addresses and data in these addresses that are changed (use decimal values for address and data!).

## Question 7 (2 + 2 = 4 points)

The state of a synchronous state machine is:

| Present state | Next state | | Output Z | |
|---|---|---|---|---|
| | $\bar{X}$ | $X$ | $\bar{X}$ | $X$ |
| S0 | S0 | S1 | 0 | 1 |
| S1 | S2 | S1 | 0 | 1 |
| S2 | S0 | S2 | 0 | 1 |

For the encoding of this state machine two D flip-flops are used (F1, F0) with S0=00, S1=10, S2=11.

Give a minimal SOP form for the data input of flip-flop F1 (i.e. DF1=f(X,F1,F0))

Give a minimal SOP form for the output Z

## Question 8 (3 points)

The ARC processor is extended with the instruction FUN. The number representation is twos complement.

FUN %rx, %ry,%rz with %rz←%rx+2×%ry
The *condition codes* may change.
%rx, %ry and %rz are registers in the registerfile (%r0 until %r31).

The instruction format is:
op=10, rd=%rz, op3=000111, rs1=%rx, bit13=0, rs2=%ry

Give an efficient micro-program for instruction FUN. If you do not know the start address you have to use 600. From the visible registers of the register file only the register indicated with %rz may change. When the instruction is finished a jump is made to address 2047 (decimal).
Use symbolic names in the fields (e.g. in field A %r6 instead of 00110). Fields that are not used must be marked with '-' (don't care). If you need more than 3 micro-instructions the maximum score for question c) is 1 point.

| address | A | Amux | B | Bmux | C | Cmux | Rd | Wr | ALU | Cond | Jump addr |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |

Name: .....

## Question 9 (3 x 1 = 3 points)

a) What type of memory needs to be refreshed? Why?

b) What is the fundamental concept behind the 'von Neumann' machine?

c) Define "programmed I/O".

## Question 10 (1 points)

A computer system is interfaced to three devices: a printer, a disk, and a display. The characteristics of the devices are summarized in the following table.

| Device | Interrupt service time | Interrupt frequency |
|---|---|---|
| Printer | 1000 us | 1/(4000 us) |
| Disk | 125 us | 1/(1000 us) |
| Display | 100 us | 1/(1000 us) |

A program P, which performs only computation (no input/output), takes 100 s to run when no input/output is being performed. How long will it take for P to run when all of the above devices are operating at their maximum speeds?

## Question 11 (2 + 2 = 4 points)

An 'embedded' microcontroller is used to control a heating system and has 8 address pins (A0 to A7), an 8 bit databus and uses 'I/O-mapped' I/O. To select the I/O space, M/In is driven low.

Within the I/O space gas burners and water pumps can be addressed with the following specifications:

Gas burners 32 Bytes at the lowest addresses of the address range.

Water pumps: 16 Bytes directly following the address range of the gas burners..

Because of security reasons, within the I/O space shadowing is not allowed.

The select lines for these areas are respectively *SelBurn* and *SelWater*. These select lines are a function of a selection of address lines and the signal M/In.

a) Give the **minimal** expression for *SelBurn* (as a function of the addresslines and M/In).

SelBurn =

b) Give the expression for *SelWater* (as a function of the addresslines and M/In).

SelWater =

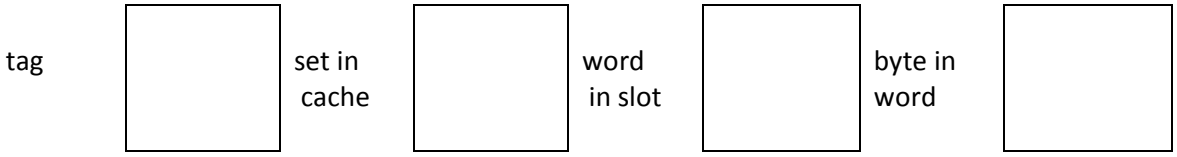
Name: .....

## Question 12 (1 + 2 + 2 + 2 = 7 points)

A 16-bits microprocessor has an on-chip primary cache with the following characteristics:

**Address space**: 4 GB, Byte-addressing
**Primary cache**: Size: 64 kB (excluding tags)
Slotsize: 16 B
Organisation: 2-way set-associative

For the primary cache, a byte-address is split into parts that are used for, respectively, comparison with the tag in the cache, selection of a set in the cache, selection of a word in a slot and selection of a byte in a word. Which bitnumbers belong to each of these parts?




## Question 13 (1 point)

A program is running on a pipelined computer in which every fifth instruction is a jump (or a branch), and there is a 30% probability that each jump is taken. When a jump is taken, the pipeline is flushed, which has a branch penalty of 2. Compute the average instruction time in terms of instruction cycles.