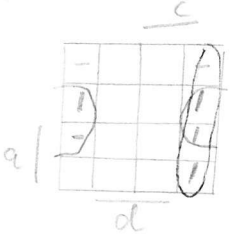
25/9/2020

1)



$b\cdot\bar{d} + c\cdot\bar{d}$ (b)

2) $y = \overline{\bar{c} + a\cdot b}$ (d)

$= \bar{\bar{c}} \cdot \overline{a\cdot b}$

$= c\,(\bar{a}+\bar{b})$

$= c\cdot\bar{a} + c\cdot\bar{b}$

3) $F(P,Q,R) = P\cdot Q'$

$= PQ'R + PQ'R'$

5 4

$\Sigma m(4,5)$ (d)

4) $\overline{\overline{a+b}} \Rightarrow a+b$

$\Rightarrow \bar{a}\cdot\bar{b}$

$\Rightarrow \overline{a\cdot a}\cdot\overline{b\cdot b}$

(3) (c)

5) 65 hex (c)

0110 0101

6) sign | exp 4 bits excess 10 | fraction 5 bit

$\cdot 1xxxxx$ hidden bit (a)

0 1010 .110000

$+ \quad 2^{10-10} \cdot 0.75 = 0.75$

7) $4\frac{3}{4}$ $0.5 \le \text{fraction} < 1$

100.11 =

$\cdot 10011 \cdot 2^{3}$

fraction $3_{10} = 13$

1101 (a)

0 1101 00110

8) 000, 011, 110, 000 (b)

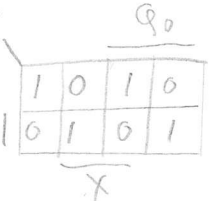
9)

PS	NS x=0	NS x=1	y
S0	S3	S1	0
S1	S0	S2	1
S2	S1	S3	1
S3	S2	S0	0

$\Rightarrow$

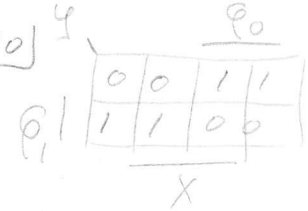
Q_1	Q_0	X	Q_1^+	Q_0^+	y
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	0	0	0

$\Rightarrow$ DF_1



$DF_1 = \bar{Q}_1\cdot\bar{Q}_0\cdot X + \bar{Q}_1\cdot Q_0\cdot X + Q_1\cdot\bar{Q}_0\cdot X + Q_1 Q_0\cdot\bar{X}$ (d)

10)



$y = \bar{Q}_1\cdot Q_0 + Q_1\cdot\bar{Q}_0$ (a)

11) c)

12) c)

13) $t_{su} = 1ns$ $t_{XOR} = 2.5ns$

$t_h = 2ns$ $t_{INV} = 1ns$

$t_{co} = 1.5ns$

a) input must be stable $2.5ns + 1ns = 3.5ns$ before active edge until $t_h - t_{xor} = 1 - 2.5 = -1.5ns$ after rising edge

3.5 ns befor and 1.5ns befor. X

b) $t_{co} + t_{XOR} + t_{su}$ critical path

$1.5ns + 2.5ns + 1ns = 5ns$ $f_{max} = \frac{1}{5ns} = 200MHz$

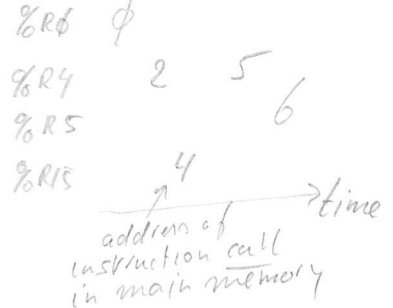
c) y can chang $1.5ns + 1ns = 2.5ns$ after active edge

d) not correct (b)

14) a) ORN %R1,%R1 $\Rightarrow$ %R1 or $\overline{\%R1} \Rightarrow$ 1111...1 (a)

15) The index in series is not increment (ie. addc %R1,4,%R1) so each loop iteration the value 6 in read $\Rightarrow$ infinite. (d) (is missing)

16)



(c)

17) (c)

on micro addr 1792 %temp = 4 * RS1

1793 %Rd = %temp + RS

18) (d)

19) word size 64 bits ⇒ 8 bytes

⇒ 8 memory addresses in main memory. $8 = 2^3$ lowest 3 bits ∅ for aligned address

.....22..22 000

(c)

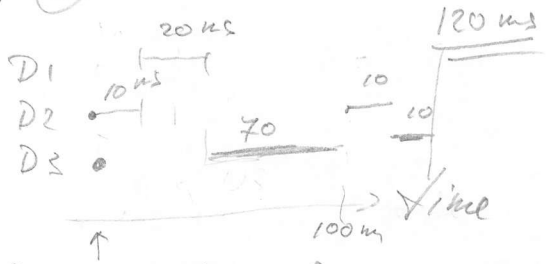
c) 13487848

1000

20) (c)

21) (d)

22) (a)



Req D3 and Req D2

D2 has higher priority

answer c is not correct.

max. freq. in 1 sec

D1: 5 × 20 ms = 100 ms

D2: 10 × 10 ms = 100 ms

D3: $\frac{1000}{800}$ × 80 ms = 100 ms

300 ms

⇒ 30 %

23)

8 MB = 2^{23} 22 ..... ∅

shadowing allowed!

(d)

Seth = $\overline{A_{22}} \cdot \overline{M_{in}}$

24) Selwifi = $A_{22} \cdot \overline{M_{in}}$ (a)

25)

address space 8MB = 2^{23} ⇒ 22 0

wordsize 4 Bytes = 2^2 ⇒ 1 0

slotsize 1kB = 2^{10} ⇒ 9 ... 0

cache size 16 kB, 2 way associative

$\frac{16kB}{2} = 8kB = 2^{13}$ 12 0

tag | set | word byte

12 11 10

(b)

26) chip, 32M × 4 bit

memory 1024 MB

word width 32 bit

chip width 4 required with 32 ⇒ $\frac{32}{4} = 8$ columns

$\frac{1024\,MB}{4\,B} = 256M$ ⇒ $\frac{256M}{32M} = 8$ Rows

chip.

(a)

27)

virtual address ⇒ 31 ..... ∅

page size 4kB = 2^{12} ⇒ 11 ..... ∅

TLB has 32 page table entries.

2-way associative

$\frac{32}{2} = 16$ sets = 2^4

15 12 11 ... 0

16 bit for key

(c)