UNIVERSITY OF TWENTE.

Exam Computer Systems/Computer Architecture and Organisation

Bachelor 2nd year, EE and CS, EWI

Module/course code: Computer Systems for **CS** (202001030)
Computer Systems for **EE** (202001136)
Date: 25 September 2020
Time: 13:45-15:30 *(+25% for students who may use extra time)*
Module-coördinator: E. Molenkamp
Instructor: E. Molenkamp / A.B.J. Kokkeler

Type of test: Closed book
Allowed aids during the test: Writing materials, simple calculator

27 questions, 9 pages and 4 pages with the ARC documentation (at the end of this document)

Instructions for this examination:

1. **If you finish before 15:15, you can quietly leave (do not leave between 15:15 and 15:30). After 15.30 you must remain seated until you are requested to come. Keep always 1.5m distance.**
2. Scientific or graphical calculators, laptops, mobile phones, books etc. are not allowed. Put those in your bag now (and **switched off**)!
3. Write your answers on this paper, in the provided boxes, and hand in this exam **and** the multiple choice form (even when you did not answer any questions).
4. Do not hand in scrap paper. It is not included in the assessment.
5. All multiple choice questions have exactly one correct answer; place an X in the correct box in this form **and** copy the answer to the multiple choice form.
6. The multiple choice form is scanned and automatically corrected. **Make sure to fill in that form completely** (except for the "docent / teacher" part).
7. For grading the exam, correction for guessing is used. **No answer given is counted as an incorrect answer**.
8. Write your name, student number and educational programme at the bottom of this page.
9. The documentation refers to the ARC processor
10. **Tip**: write your answers on scrap paper. After the exam the answers are published.

You can score a total of 27 points for this exam; you need 17 points to pass the exam.

Symbols logical operators:
not a is also represented as $\overline{a}$, **a'**, **!a**, **#a**
a and b is also represented as **a.b**, **a&b**
a or b is also represented as **a + b**
a xor b is also represented as $a \oplus b$

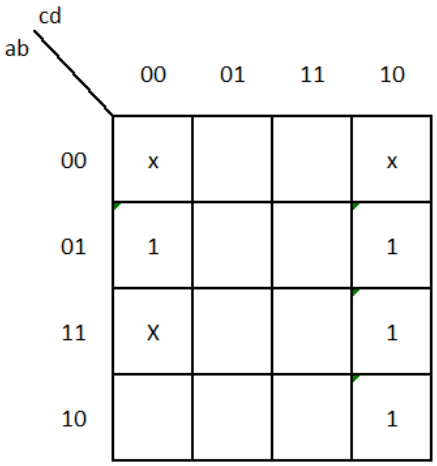
Please underline your family name (i.e., the name on your student card)

Name: .....

Student number: .....

Educational programme (EE, TCS, ..): .....

Question 1



What is a simplified Boolean equation for this Karnaugh map?
'X' denotes a don't care term and the fields that are not filled are 0.

a☐ d + a.c'

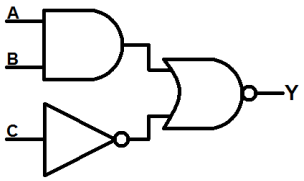
b☐ b.d' + c.d'

c☐ a'.b.d' + a.c.d'

d☐ d'.(a' + b' + c)

Question 2

What is the simplified Sum of Products of the Boolean expression for this design:



a☐ A'.B'.C'

b☐ A.B + C'

c☐ A' + B' + C'

d☐ A'.C + B'.C

Question 3

What is the minterm expansion of F(P,Q,R) = P.Q'

a☐ $\sum m(1,2)$

b☐ $\sum m(2,3)$

c☐ $\sum m(3,4)$

d☐ $\sum m(4,5)$

Question 4

A two-input OR gate is to be realized with only two-input NAND gates. What is the minimum number of two-input NAND gates?

a☐ 1

b☐ 2

c☐ 3

d☐ 4

Question 5

What is the binary representation of the hexadecimal number 65 ?

a☐ 100001

b☐ 110101

c☐ 01100101

d☐ None of these

Question 6

Given is a normalized floating point representation in base 2. The bit pattern from left to right is: Sign bit: 1 bit (1 is negative, 0 is positive), Exponent field: 4 bits in excess 10, Fraction field: 5 bits (not included is the hidden bit). Point is left of hidden bit.
Only when the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

What is the decimal value of the pattern
0 1010 10000
for this floating point representation?
(spaces are added for readability)

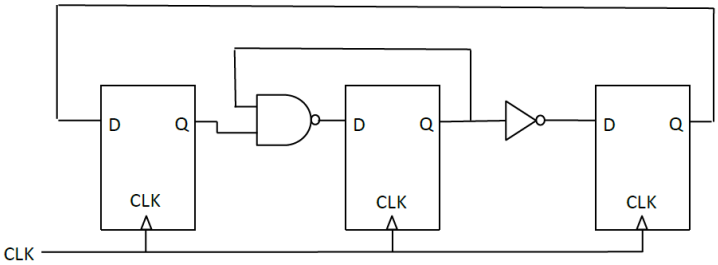
a☐ 0.75
b☐ 1
c☐ 1.5
d☐ 2^{10}

Question 7

What is the bit representation of decimal $4\frac{3}{4}$ (use rounding style truncation) in the floating point representation of question 6?

a☐ 0 1101 00110
b☐ 0 1000 11000
c☐ 0 1111 00100
d☐ None of these

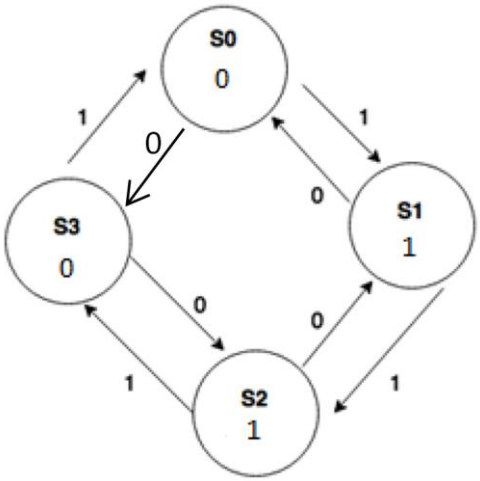
Question 8



The flip-flops in this schematic are positive edge triggered Data flip-flops. The values of the flip-flips are initially all 0. After how many clock cycles will the system will be again in the state that all flip-flops are 0?

a☐ 2 clock cycles
b☐ 3 clock cycles
c☐ 4 clock cycles
d☐ more than 4 clock cycles.

Question 9



This finite state machine of this Moore machine is realized with 2 data flip-flops (Q_1Q_0) (note: Q_1 is left bit of the state) and combinational logic. The input is X and the output is Y. The encoding of the states is:

state	Q_1	Q_0
S0	0	0
S1	0	1
S2	1	0
S3	1	1

What is a simplified Boolean expression for the combinational logic for the input of flip-flop Q_1 (=D_1).

a☐ $D_1 = Q_1' + X'$

b☐ $D_1 = Q_0 + Q_1'.X$

c☐ $D_1 = Q_1'.X + Q_1.Q_0'.X' + Q_1'.Q_0.X$

d☐ $D_1 = Q_1'.Q_0'.X' + Q_1'.Q_0.X + Q_1.Q_0'.X + Q_1.Q_0.X'$

Question 10

Given is the finite state machine of question 9. What is a Boolean equation for the output Y?

a☐ $Y = Q_1'.Q_0 + Q_1.Q_0'$

b☐ $Y = Q_1.Q_0.X + Q_1.Q_0'.X$

c☐ $Y = Q_1' + Q_0'$

d☐ Y = None of these

Question 11

For a Mealy machine the output depends on:

a☐ only the present state

b☐ only the previous state

c☐ the present state and the input

d☐ only the input

Question 12

What is a Boolean equation for the output *carry* of a full adder with inputs *a*, *b* and *cin*?

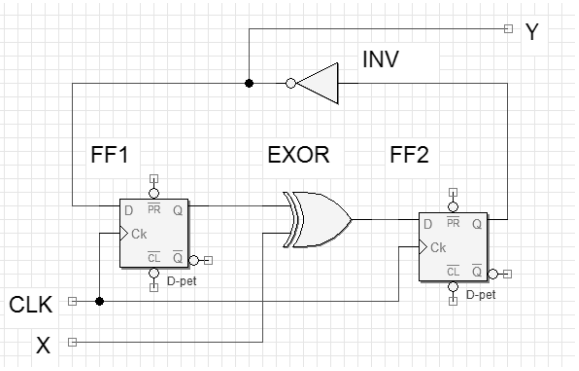
a☐ $a \oplus b \oplus cin$

b☐ a + b + cin

c☐ a.b + a.cin + b.cin

d☐ a.b.cin

Question 13



For this circuit the asynchronous low active inputs $\overline{PR}$ and $\overline{CL}$ are connected to 1 (i.e. normal operation of the D flip flops).
For both flip flops the setup time is 1ns, the hold time is 2ns and the flip flop clock to output delay is 1.5ns. The delay of the EXOR is 2.5ns (for both inputs to output). The delay of the INV is 1ns. Other delays are negligible

Which statement is true?

a☐ Input X must be stable 1ns before the rising edge of CLK until 2 ns after the rising edge of CLK.

b☐ The maximum clock frequency for a correct operation is 200 MHz.

c☐ Output Y is stable 2ns after the rising edge of CLK until the next rising edge of CLK.

d☐ The output Y is always 1.

Question 14

Which ARC assembly instruction will change the contents of register %r1 to decimal -1?
Note: the ARC tools uses twos complement representation for numbers.

a☐ orn %r1, %r1, %r1

b☐ ld [%r0-1], %r1

c☐ sethi -1, %r1

d☐ none of these

Question 15

```
        .begin
        .org 0
        sethi   series,%r1
        srl     %r1,10,%r1
        addcc   %r0,%r0,%r11
lp:     ld      [%r1], %r2
        addcc   %r2,%r0,%r0
        be      rdy
        addcc   %r11,%r2,%r11
        ba      lp
rdy:    halt
series: 6,  7, 8, -1, 0, 0
        .end
```

Initial values of the registers in the register file are decimal 0.
Which statement is true?

a☐ After execution series is changed in decimal 12, 14, 16, -2, 0, 0

b☐ After execution the contents of %r11 is decimal 6

c☐ After execution the contents of %r11 is decimal 20

d☐ The loop in the program is infinite

Question 16

```
        .begin
        .org 0
        addcc   %r0, 2, %r4
        call    lbl
        addcc   %r4, 1, %r5
rdy:    halt
lbl:    addcc   %r4, 3, %r4
        jmpl    %r15, 4, %r0
        .end
```

a☐ contents of %r4 is decimal 2

b☐ contents of %r5 is decimal 3

c☐ contents of %r15 is decimal 4

d☐ contents of %r15 is decimal 8

After execution of this program, which statement is true?

Question 17

The ARC processor is extended with instruction FUN with the RTL description
$R[rd] \leftarrow 4 \times R[rs1] + R[rs2]$ (e.g. *fun %r3,%r1, %r6* results in $\%r6 \leftarrow 4 \times \%r3 +$ %r1)
What is a correct micro program for the execution phase of this instruction?

a☐

address	A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
1792	-	1	-	1	-	1	0	0	addcc	next	-
1793	-	1	%temp0	0	-	1	0	0	addcc	jump	2047

b☐

address	A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
1792	-	1	%r0	0	%temp0	0	0	0	addcc	next	-
1793	-	1	%temp0	0	%temp0	0	0	0	addcc	next	-
1794	%temp0	0	-	1	-	1	0	0	addcc	jump	2047

c☐

address	A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
1792	-	1	%r0	0	%temp0	0	0	0	Lshift2	next	-
1793	%temp0	0	-	1	-	1	0	0	addcc	jump	2047

d☐

address	A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
1792	-	1	%r0	0	%temp0	0	0	0	addcc	next	-
1793	%temp0	0	%temp0	1	-	1	0	0	addcc	jump	2047

Question 18

Which statement is true for the ARC processor?

a☐ The micro program of each instruction ends with incrementing the program counter with decimal 4.

b☐ All instructions are executed in 1 clock cycle.

c☐ The program counter counts the number of executed instructions of a program.

d☐ None of these.

Question 19

Given is a processor with word size of 64 bits. Main memory is byte organized and has 32 address bits.
What is the correct aligned address (hexadecimal notation is used)?

a☐ A123FA12

b☐ BDEF1234

c☐ 13487848

d☐ None of these.

Question 20

Which statement is true?

a☐ A DRAM memory cell is larger than an SRAM memory cell and a SRAM memory cell needs to be refreshed.

b☐ A DRAM memory cell is smaller than an SRAM memory cell and a SRAM memory cell needs to be refreshed.

c☐ A DRAM memory cell is smaller than an SRAM memory cell and a DRAM memory cell needs to be refreshed.

d☐ A DRAM memory cell is larger than an SRAM memory cell and a DRAM memory cell needs to be refreshed.

Question 21

Which statement is true?

a☐ If a Daisy Chain connection is used for bus arbitration then all connected devices have the same priority to use the bus.

b☐ The fully centralized bus arbitration is the most flexible solution because the number of connected devices is unlimited.

c☐ In all computers the CPU and the devices are connected to the same physical bus.

d☐ In *I/O-mapped I/O*, addresses assigned to memory locations can also be assigned to I/O devices.

Question 22

A computer must service three devices whose interrupting frequencies, service times, and assigned priorities are given in the table below.

Device	Service time	Maximum Frequency	Priority
D1	20 ms	1/(200 ms)	3 (highest)
D2	10 ms	1/(100 ms)	2
D3	80 ms	1/(800 ms)	1 (lowest)

Assume that a higher priority device can interrupt a lower priority device.

What is correct?

a☐ For device D3 the worst case time between its service request and the completion of its service is 120 ms

b☐ For device D3 the worst case time between its service request and the completion of the service is 30 ms

c☐ When all devices operate at their maximum frequency the processor requires 50% of the processor time to handle these services

d☐ none of the above

Question 23

An embedded computer system has a physical address space of 8 MB. The memory is byte addressable. I/O mapped I/O is used. When pin *M/in* is low the I/O devices are selected. The system contains an Ethernet controller and a Wifi controller according to the following specifications concerning addressing.

Ethernet controller: 1 MB at the lowest addresses of the address range.
Wifi controller: 4 MB at the highest addresses of the address range.
Shadowing is allowed.

The signals to select the different areas are respectively *SelEth* and *SelWifi*.
The bits of the address bus are $A_{N-1}..A_0$ (N is number of address lines, right most bit has index 0)

What is the minimal equation for *SelEth* ?

a☐ *SelEth* = $!A_{22}$ & $!A_{21}$ & $!A_{20}$ & !M/in

b☐ *SelEth* = $!A_3$ & $!A_2$ & $!A_1$ & A_0 & !M/in

c☐ *SelEth* = $!A_{23}$ & $!A_{21}$ & !M/in

d☐ *SelEth* = $!A_{22}$ & !M/in

Question 24

See question 23.

What is the minimal equation for *SelWifi* ?

a☐ *SelWifi* = A_{22} & !M/In

b☐ *SelWifi* = $!A_{22}$ & $!A_{21}$!M/In

c☐ *SelWifi* = ($!A_{22}$ + $!A_{21}$) & !M/In

d☐ *SelWifi* = !M/In

Question 25

A 32-bits microprocessor has an on-chip primary cache with the following characteristics:

Address space: 8 MB, Byte-addressing
Primary cache: Size: 16 KB (excluding tags)
Slotsize: 1KB
Organisation: 2-way set-associative

For the primary cache, a byte-address is split into parts that are used for, respectively, comparison with the *tag* in the cache, selection of a *set in the cache*, selection of a *word in a slot* and selection of a *byte in a word*.

What are the bit numbers of the address that selects **set in the cache**?
Note: the right most bit has number 0.

a☐ 13, 12, 11, 10, 9
b☐ 12, 11, 10
c☐ 11, 10, 9
d☐ 10, 9

Question 26

A dynamic RAM chip is organised as follows: 32M x 4 bits. Using multiple of these chips, a memory module of in total 1024 Mbytes has to be built. The word width is 32 bits.
How many columns (to establish the correct word width) and how many rows does the memory module contain?

a☐ columns: 8 rows: 8
b☐ columns: 8 rows: 4
c☐ columns: 4 rows: 6
d☐ columns: 32 rows: 1

Question 27

A processor generates 32-bit virtual addresses and the page size is 4 KB. A 2-way set associative Translation Look-aside Buffer (TLB) that can hold a maximum of 32 page table entries is used to accelerate address translation.
What is the TLB tag size?

a☐ 5 bits
b☐ 12 bits
c☐ 16 bits
d☐ 20 bits