UNIVERSITY OF TWENTE.

Exam Computer Systems/Computer Architecture and Organisation

Bachelor 2nd year, EE and CS, EWI

Module/course code: Computer Systems for **CS** (202001030)
Computer Systems for **EE** (202001136)
Date: 12 October 2020
Time: 9:00-10:45 *(+25% for students who may use extra time)*
Module-coördinator: E. Molenkamp
Instructor: E. Molenkamp / A.B.J. Kokkeler

Type of test: Closed book
Allowed aids during the test: Writing materials, simple calculator

27 questions, 9 pages and 4 pages with the ARC documentation (at the end of this document)

Instructions for this examination:

1. **If you finish before 10:30, you can quietly leave. Do not leave between 10:30 and 10:45. After 10:45 you must remain seated until you are requested to come. Keep always 1.5m distance.**
2. Scientific or graphical calculators, laptops, mobile phones, books etc. are not allowed. Put those in your bag now (and **switched off**)!
3. Write your answers on this paper, in the provided boxes, and hand in this exam **and** the multiple choice form (even when you did not answer any questions).
4. Do not hand in scrap paper. It is not included in the assessment.
5. All multiple choice questions have exactly one correct answer; place an X in the correct box in this form **and** copy the answer to the multiple choice form.
6. The multiple choice form is scanned and automatically corrected. **Make sure to fill in that form completely** (except for the "docent / teacher" part).
7. For grading the exam, correction for guessing is used. **No answer given is counted as an incorrect answer**.
8. Write your name, student number and educational programme at the bottom of this page.
9. The documentation refers to the ARC processor
10. **Tip**: write your answers on scrap paper. After the exam the answers are published.

You can score a total of 27 points for this exam; you need 17 points to pass the exam.

Symbols logical operators:
not a is also represented as $\overline{a}$, **a'**, **!a**, **#a**
a and b is also represented as **a.b**, **a&b**
a or b is also represented as **a + b**
a xor b is also represented as $a \oplus b$

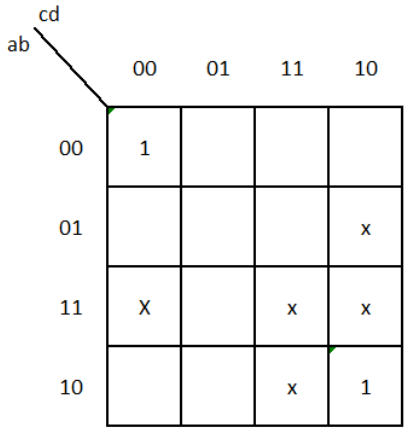
Please underline your family name (i.e., the name on your student card)

Name: .....

Student number: .....

Educational programme (EE, TCS, ..): .....

Question 1



What is a simplified Boolean equation for this Karnaugh map?
'X' denotes a don't care term and the fields that are not filled are 0.

a☐ a'.b'.c'.d' + a.c

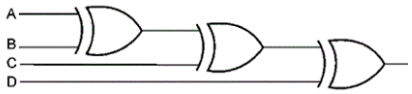
b☐ b.d' + c.d'

c☐ a'.b.d' + a.c.d'

d☐ d'.(a' + b' + c)

Question 2

Beneath is a schematic with a chain of XOR gates. Which statement is true?



a☐ The behavior of this design cannot be realized with only 2-input NAND gates.

b☐ The behavior of this design cannot be realized with only 2-input NOR gates.

c☐ The output is 1 if an odd number of input values is 1

d☐ The output is 1 if an even number of input values is 1

Question 3

What is the Boolean equation for a system that is specified with the minterm expansion F(P,Q,R)= $\sum m(0)$.

a☐ F(P,Q,R)=P'.Q'.R'

b☐ F(P,Q,R)=P' + Q' + R'

c☐ F(P,Q,R)=P.Q.R

d☐ F(P,Q,R)=P + Q + R

Question 4

$$Y = A \cdot S + B \cdot \bar{S}$$

What Boolean equation is equal to this equation?

a☐ $Y = (\bar{A} + \bar{S}).(\bar{B} + S)$

b☐ $Y = \overline{(\bar{A} \cdot \bar{S}) + (\bar{B} \cdot S)}$

c☐ $Y = \overline{(\bar{A} + \bar{S}) \cdot (\bar{B} + S)}$

d☐ $Y = \overline{(\overline{A + S}) \cdot (\overline{B + \bar{S}})}$

Question 5

Given is the two's complement number 10101. What is the decimal value?

a☐ -5

b☐ -10

c☐ -11

d☐ 21

Question 6

Given is a normalized floating point representation in base 2. The bit pattern from left to right is:
Sign bit: 1 bit (1 is negative, 0 is positive), Exponent field: 5 bits in excess 10, Fraction field: 5 bits (not included is the hidden bit). Point is right of hidden bit.
Only when the exponent field is filled with all zeros, the representation is not normalized. In that case the decimal number 0 is represented, independent of the sign and fraction field.

What is the decimal value of the pattern
1 01010 10000
for this floating point representation?
(spaces are added for readability)

a☐ -0.75
b☐ -1
c☐ -1.5
d☐ -2^{10}

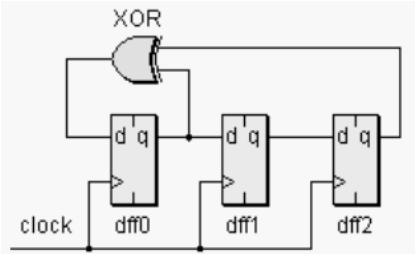
Question 7

How many representations for decimal 0 does the floating point representation of question 6 have?

a☐ 0
b☐ 2
c☐ 32
d☐ 64

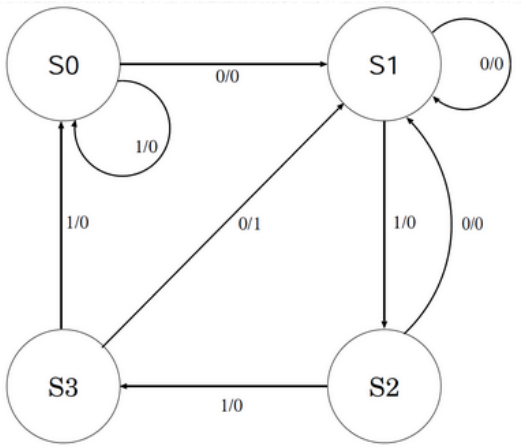
Question 8

Below is a schematic of a pseudo random generator. The flip flop outputs are the outputs of the design and the clock input is connected to an oscillator. Assume that all flip flops have initially the value 1. How many different patterns are generated?



a☐ 15
b☐ 8
c☐ 7
d☐ 3

Question 9



This finite state machine is realized with 2 data flip flops (Q_1Q_0) (Q_1 is the left bit of the state) and combinational logic. The input is X and the output is Y. The encoding of the states is:

state	Q_1	Q_0
S0	0	0
S1	0	1
S2	1	0
S3	1	1

What is a simplified Boolean expression for the combinational logic for the input of flip-flop Q_1 (=D_1).

a☐ $D_1 = Q_1' + X'$

b☐ $D_1 = Q_0 + Q_1'.X$

c☐ $D_1 = Q_1'.X + Q_1.Q_0'.X' + Q_1'.Q_0.X$

d☐ $D_1 = Q_1.Q_0'.X + Q_1'.Q_0.X$

Question 10

Given is the finite state machine of Question 9. What is a Boolean equation for the output Y?

a☐ $Y = Q_1.Q_0.X'$

b☐ $Y = Q_1.Q_0 .X' + Q_1.Q_0'Q_1 .X'$

c☐ $Y = Q_1'+Q_0'$

d☐ None of these

Question 11

Given is the finite state machine of Question 9. The encoding of the states is changed in the encoding below:

state	Q_1	Q_0
S0	1	1
S1	1	0
S2	0	1
S3	0	0

Which statement is true?

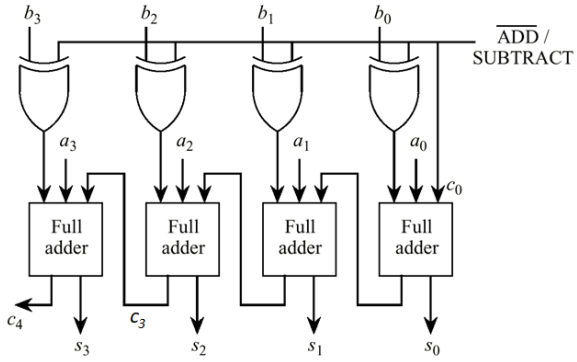
a☐ The realization does not depend on the encoding of the states.

b☐ $Y = Q_1'.Q_0'.X'$

c☐ $D_1 = 0$

d☐ The FSM is a MOORE machine

Question 12



This simple ALU can add and subtract signed numbers. $s_3..s_0$ are the sum bits and c_4,c_3 are the carry out bits. The logic for the status bits is not shown (V is oVerflow, N is Negative, Z is Zero, C is carry). Which statement is true for this logic?

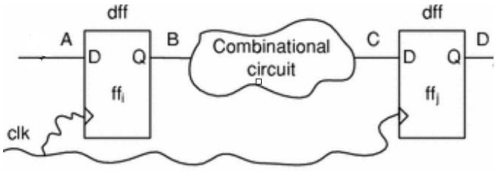
a☐ $V = c_4 \oplus c_3$

b☐ $N = c_4$

c☐ $Z = \overline{c_4 + s_3 + s_2 + s_1 + s_0}$

d☐ $C = c_3$

Question 13



For both flip flops the setup time is 0.8ns, the hold time is 1ns and the flip flop clock to output delay is 1.2ns. The delay of the combinational circuit is 2ns.
Other delays are negligible

Which statement is true?

a☐ Line C must be stable 0.8ns before the rising edge of CLK until 1ns after the rising edge of clk

b☐ The maximum clock frequency for a correct operation is 200 MHz

c☐ Line D is stable 1ns after the rising edge of CLK until the next rising edge of CLK

d☐ The right flip flop in this schematic has a hold time violation.

Question 14

Which ARC assembly instruction will change the contents of register %r1 to decimal 1?
(signed representation is used)

a☐ sethi 1, %r1

b☐ ld [%r0+1], %r1

c☐ orcc %r0, 1, %r1

d☐ orncc %r1, %r1, %r1

Question 15

What is the bit pattern of the *field op3* in the machine code of an ARC instruction when the start address in the micro store is decimal 1788?

a☐ 000000

b☐ 111111

c☐ 000010

d☐ None of these

Question 16

```
        .begin
        .org 0
        sethi   series,%r1
        srl     %r1,10,%r1
        addcc   %r0,%r0,%r11
lp:     ld      [%r1], %r2
        addcc   %r2,%r0,%r0
        be      rdy
        addcc   %r11,%r2,%r11
        addcc   %r1,4,%r1
        ba      lp
rdy:    halt
series: 6, 7, 8, -1, 0, 0
res:    13
        .end
```

Which statement is true?

a☐ After execution the contents of %r11 is decimal 20

b☐ After execution the contents of %r11 is decimal -1

c☐ After execution the contents of %r11 is decimal 6

d☐ the loop in the program is infinite

Question 17

In computer science, self-modifying code is code that alters its own instructions while it is executing. The program below is an example.
Note: the data at address with label `fun` is in hexadecimal notation.
After execution of this program, which statement is true?

```
        .begin
        .org 0
        addcc %r0,-1,%r1
        ld [24],%r2
        st %r2,[12]
        addcc %r0, %r0, %r0
        addcc %r0,1,%r1
rdy:    halt
fun:    10800002h
        .end
```

a☐ contents of %r1 is decimal -1

b☐ contents of %r1 is decimal 1

c☐ contents of %r2 is decimal -1

d☐ contents of %r2 is decimal 1

Question 18

A	Amux	B	Bmux	C	Cmux	Rd	Wr	ALU	Cond	Jump addr
100101	0	000000	1	100101	0	0	0	1110	110	00000000000

Given is a micro instruction of the ARC processor. Which statement is true?

a☐ The data in the register file is not changed

b☐ The program counter is incremented with 4

c☐ The instruction register is incremented with 4

d☐ Only if the status bit Z (Zero) is set a jump is made to micro address decimal 0

Question 19

What is statement is correct?

a☐ The register in a processor with name *program counter* counts the number of instructions executed.

b☐ A computer based on the *von Neumann model* has no Control Unit.

c☐ A processor that supports memory-mapped I/O has different read and write instructions for IO and memory.

d☐ Memory-mapped I/O uses a single address space to address both memory and I/O devices .

Question 20

Given two processors with word size of 16 bits and a byte-organized memory. Processor A uses Little-Endian addressing and Processor B uses Big-Endian addressing. Processor A writes data to memory and processor B reads data from the address written by Processor A. What is read by processor B when processor A wrote (hex) 89AB?

a☐ 89AB

b☐ AB89

c☐ BA98

d☐ A98B

Question 21

What is correct?

a☐ In the interrupt I/O technique the processor is polling for an interrupt of a device

b☐ In the interrupt I/O technique the processor interrupts the connected devices

c☐ DMA is a technique for transferring data between main memory and external device with minimal involvement of the CPU.

d☐ none of the above

Question 22

Consider the following interrupt scenario. An interrupt **cannot** suspend other interrupts:

Task	Service time	Maximum allowed latency	Maximum Frequency
A	10 ms	15 ms	1/(100 ms)
B	20 ms	35 ms	1/(200 ms)
C	40 ms	200 ms	1/(400 ms)
D	50 ms	200 ms	1/(500 ms)

What is correct?

a☐ Maximum allowed latencies for all the tasks are met

b☐ Task A can prevent task C being serviced in time

c☐ Task D can prevent task A being serviced in time

d☐ none of the above

Question 23

An embedded computer system has a physical address space of 16 MB. The memory is byte addressable. I/O mapped I/O is used. When pin *M/in* is low the I/O devices are selected. The system contains an Ethernet controller, video-RAM and a Wifi controller according to the following specifications concerning addressing.

Ethernet controller:	1 MB at the lowest addresses of the address range.
Video-RAM:	512 KB directly following the area for the Ethernet controller.
Wifi controller:	4 MB at the highest addresses of the address range.

Shadowing is not allowed.

The signals to select the different areas are respectively *SelEth*, *SelVideo* en *SelWifi*.
The bits of the address bus are $A_{N-1}..A_0$ (N is number of address lines, right most bit has index 0)

What is the equation for *SelEth* ?

a☐ *SelEth* = $!A_{22}$ & $!A_{21}$ & $!A_{20}$ & !M/in

b☐ *SelEth* = $!A_{23}$ & $!A_{21}$ & $!A_{20}$ & !M/in

c☐ *SelEth* = $!A_{23}$ & $!A_{22}$ & $!A_{21}$ & $!A_{20}$ & !M/in

d☐ *SelEth* = $!A_3$ & $!A_2$ & $!A_1$ & A_0 & !M/in

Question 24

See question 23.

What is the equation for *SelVideo* ?

a☐ *SelVideo* = $!A_{23}$ & $!A_{22}$ & A_{21} & $!A_{20}$ & $!A_{19}$ & !M/In

b☐ *SelVideo* = $!A_{23}$ & $!A_{22}$ & $!A_{21}$ & A_{20} & $!A_{19}$ & !M/In

c☐ *SelVideo* = ($!A_{22}$ + $!A_{21}$ + A_{20} + $!A_{19}$ + $!A_{18}$ +$!A_{17}$) & !M/In

d☐ none of the above

Question 25

A 16-bits microprocessor has an on-chip primary cache with the following characteristics:

Address space:	4 MB, Byte-addressing
Primary cache:	Size: 32 KB (excluding tags)
	Slotsize: 1KB
	Organisation: 4-way set-associative

For the primary cache, a byte-address is split into parts that are used for, respectively, comparison with the *tag* in the cache, selection of a *set in the cache*, selection of a *word in a slot* and selection of a *byte in a word*. Note: the right most bit has number 0.

What are the bit numbers of the address that selects **set in the cache**?

a☐ 13, 12, 11, 10, 9

b☐ 12, 11, 10

c☐ 11, 10, 9

d☐ none of the above

Question 26

See question 25

What are the bit numbers of the address that selects **word in slot**?

a☐ 7, 6, 5, 4, 3, 2, 1

b☐ 8, 7, 6, 5, 4, 3, 2, 1

c☐ 9, 8, 7, 6, 5, 4, 3, 2, 1

d☐ 9, 8, 7, 6, 5, 4, 3, 2

Question 27

A dynamic RAM chip is organised as follows: 64M x 2 bits. Using multiple of these chips, a memory module of in total 1024 Mbytes has to be built. The word width is 32 bits.
Multiple of these chips are placed on a grid where the number of columns defines the word-width and the overall memory capacity is determined by the number of rows. How many columns and how many rows does the memory module contain?

a☐ columns: 16 rows: 8

b☐ columns: 16 rows: 4

c☐ columns: 32 rows: 4

d☐ columns: 8 rows: 8