Question 1

25 points

(a) Convert the decimal number -15 to a 6-bit 2-complement binary number. First give your final answer (the binary number):

Briefly explain your answer.

Word count: 0, character count: 0

(b) Convert the (unsigned) binary number 01001101100 to hexadecimal; first give the f

Briefly explain your answer.

Word count: 0, character count: 0

(c) Convert the hexadecimal number 2A8 to decimal; first give the fina

Briefly explain your answer.

Word count: 0, character count: 0

(d) Suppose we make a new number system for 4-digit binary numbers, by giving the bits, from left to right, the following weights: 2, 4, 2, 1. What can we say about this?

A ○ With this system, we can represent all integers from 0 to 9, and each of them in only one way.
D ○ This is useless because the weights should all be different.
B ○ With this system, we can represent some, but not all integers from 0 to 9.
E ○ This is useless because it cannot represent negative numbers.
C ○ With this system, we can represent all integers from 0 to 9, and some of them can be represented in multiple ways.

(e) Given a 5-bit, 2-complement, binary number, which of the following operations multiplies it by -1 ?

D ○ First add the binary number 00001 to it, and then invert all bits.
C ○ First invert all bits and then add the binary number 00001 to it.
A ○ Shift to the right by 1 position, dropping the right-most bit, and inserting a 0 at the left.
E ○ Shift to the left by 1 position, dropping the left-most bit, and inserting a 0 at the right.
B ○ Invert all bits.

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Question 2

25 points

(a) Give the truth table of a 3-input OR/XOR-gate: if input A=1, the output D is the OR of inputs B and C, otherwise, it is the XOR o C.The XOR ("exclusive OR") of two inputs is 1 if one of the inputs is 1, but not both.
(You may not need all rows in the table; leave any unused rows blank.)

	A	B	C	D
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

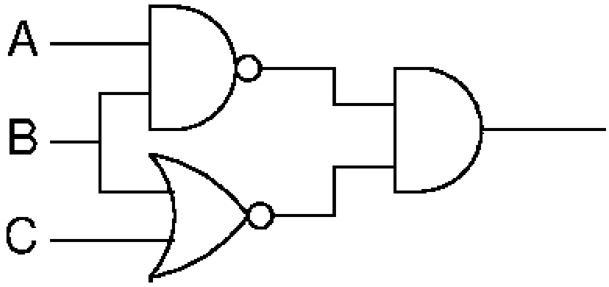
The editable cells are marked in light yellow.

(b) In the left-most column of the below table, we give a derivation in Boolean algebra, starting with $(A+\overline{A})\cdot\overline{AB}\cdot\overline{C}$, making one step per row.
Indicate in each row, which rule of Boolean algebra is used to make that step. Choose “wrong” if you think that that step is not c possible that a rule is used multiple times, or not at all, in this derivation; however, each step uses only a single rule.)

To clarify this, in the first row you should indicate which Boolean algebra rule is used to demonstrate that the formula on that row $1\cdot\overline{AB}\cdot\overline{C}$, follows from our starting formula $(A+\overline{A})\cdot\overline{AB}\cdot\overline{C}$. The second row should indicate how the formula on the second row follows from the formula on the first row, and so on.

	wrong	DeMorgan	distributive	commutative	identity	complement	associative
	J	I	F	L	H	G	K
$=1\cdot\overline{AB}\cdot\overline{C}$	○	○	○	○	○	○	○
$=\overline{AB}\cdot\overline{C}$	○	○	○	○	○	○	○
$=\overline{A}\cdot\overline{BC}$	○	○	○	○	○	○	○
$=\overline{A+BC}$	○	○	○	○	○	○	○
$=\overline{(A+B)\cdot(A+C)}$	○	○	○	○	○	○	○

(c) Describe the operation of the following logic circuit as a formula in Boolean logic.
Note: Boolean formulas often have a bar above part of the equation. If this is the case in your formula, you can either use the bu editor to type this (accessible via the ∑ button), or simply type something like not(ABC) or /(ABC), as long as it's clear what you r



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(d) Suppose we take a 2-input OR gate, and put inverters at its inputs and at its output. What do we get?

B ○ OR gate

C ○ NAND gate.

D ○ AND gate.

A ○ NOR gate.

E ○ None of the above.

Flag this question

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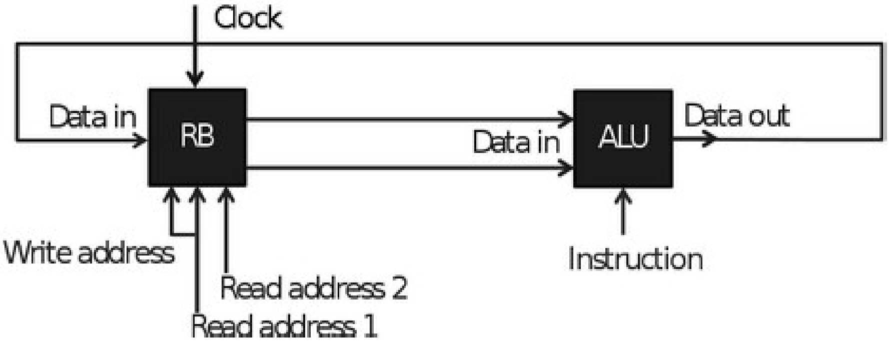
Question 3

12 points



The ALU of the processor above has two instructions: 0 = 'ADD' and 1 = 'MUL'.
The register bank (RB) contains four 8-bit registers.
Initially R1, R2 and R3 contain some numbers x, y and z, respectively.
Give for this processor the program for computing $xy + xz + x$ and storing the result in R1.
(You may not need all timeslots.)

	A	B	C	D
1		read address 1 / write address	read address 2	instruction
2	Timeslot 0			
3	Timeslot 1			
4	Timeslot 2			
5	Timeslot 3			
6	Timeslot 4			

The editable cells are marked in light yellow.

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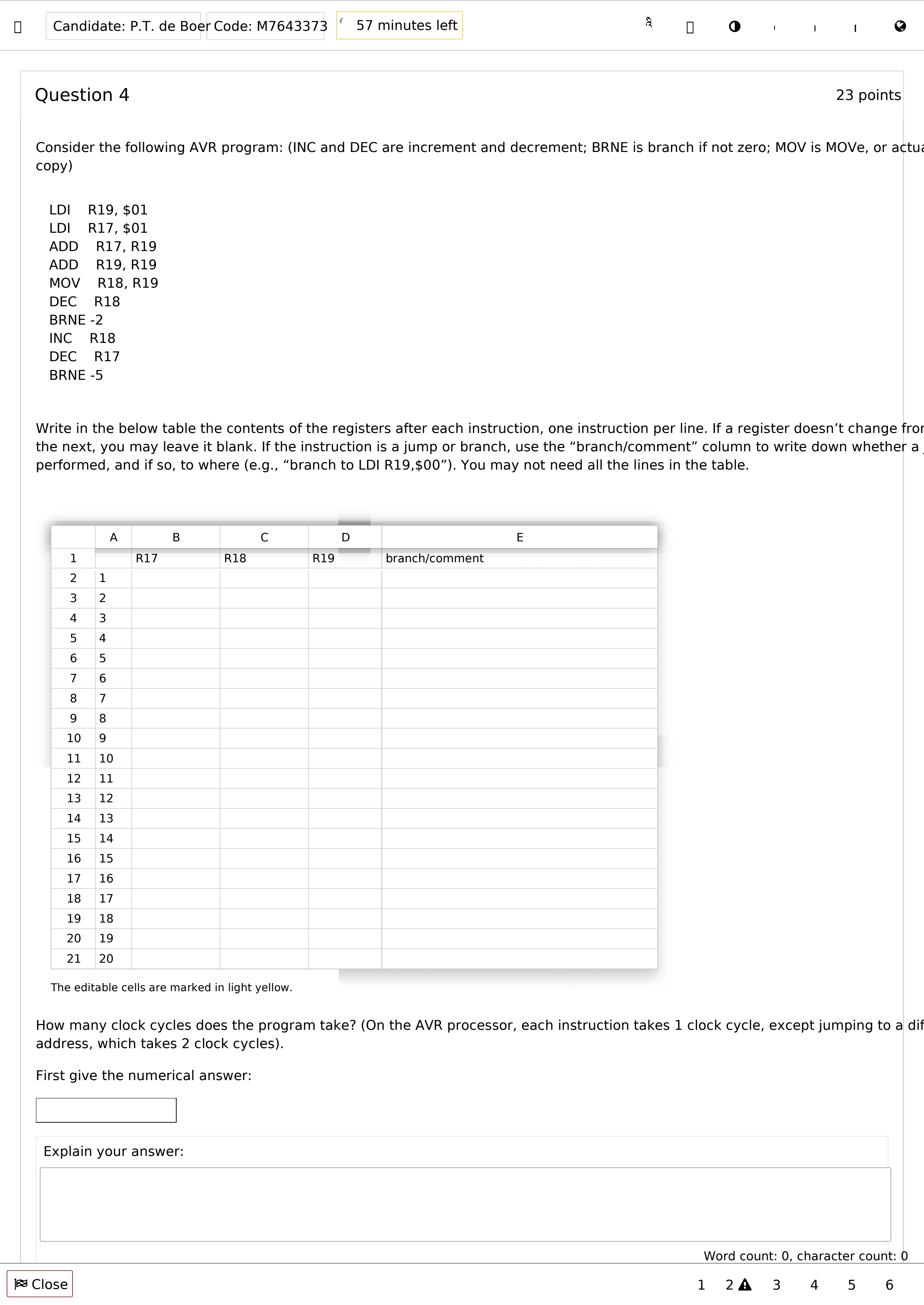

Question 4

23 points

Consider the following AVR program: (INC and DEC are increment and decrement; BRNE is branch if not zero; MOV is MOVe, or actua
copy)

```
LDI    R19, $01
LDI    R17, $01
ADD    R17, R19
ADD    R19, R19
MOV    R18, R19
DEC    R18
BRNE -2
INC    R18
DEC    R17
BRNE -5
```

Write in the below table the contents of the registers after each instruction, one instruction per line. If a register doesn't change fror
the next, you may leave it blank. If the instruction is a jump or branch, use the "branch/comment" column to write down whether a
performed, and if so, to where (e.g., "branch to LDI R19,$00"). You may not need all the lines in the table.

	A	B	C	D	E
1		R17	R18	R19	branch/comment
2	1				
3	2				
4	3				
5	4				
6	5				
7	6				
8	7				
9	8				
10	9				
11	10				
12	11				
13	12				
14	13				
15	14				
16	15				
17	16				
18	17				
19	18				
20	19				
21	20				

The editable cells are marked in light yellow.

How many clock cycles does the program take? (On the AVR processor, each instruction takes 1 clock cycle, except jumping to a dif
address, which takes 2 clock cycles).

First give the numerical answer:

Explain your answer:

Word count: 0, character count: 0

Question 5

15 points

What is the mathematical function that is computed by the code below?
Assume that X and Y are positive; the final result is in R19.

(You may not have seen the BRCC instruction before: it's BRanch if Carry Clear, so it jumps if the previous instructi
set the carry flag, i.e., did not result in an overflow (in addition) or negative number (in subtraction).)

```
    LDI  R17, $X
    LDI  R18, $Y
    LDI  R19, $00
  repeat:
    INC  R19
    SUB  R17, R18
    BRCC repeat
    DEC  R19
```

Write as a function of X and Y, e.g. f(X, Y) = X + Y:

Explain your answer:

Word count: 0, character count: 0

Flag this question

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